## REMARKS

This Amendment responds to the Office Action dated September 27, 2004 in which the Examiner rejected claims 13-18 under 35 U.S.C. §112, second paragraph and rejected claims 13-24 under 35 U.S.C. §103.

As indicated above, claim 13 has been amended in order to correct a typographical error. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 13-18 under 35 U.S.C. §112 second paragraph.

Claims 13, 17-19, 23 and 24 were rejected under 35 U.S.C. §103 as being obvious over *Shou et al.* (U.S. Patent No. 5,811,859) in view of *Bergemont* (WO 94/29898).

*Shou et al.* appears to disclose in FIG. 3, a LSI pattern of inverted amplifier INV consisting of 3 stages MOS invertors, I1, I2 and I3. For the invertors I1 and I2, there are shaped a common P-type semiconductor layer PL1 and a common N-type semiconductor layer NL1. P-type semiconductor layer PL2 and N-type semiconductor layer NL2 are shaped for I3. Drain voltage Vdd and source voltage Vss are connected to PL1 and NL1 through contacts C1 and C2. A contact is a metal part passing through in semiconductor layer in the direction of thickness, for electrical connection. The drain voltage Vdd and source voltage Vss are connected to PL2 and NL2 through contacts C7 and C8. The semiconductor layers PL1 and NL1 are provided with contacts C3 and C4 for an output from the first stage, respectively, and are provided with contacts C5 and C6 for an output from the second stage, respectively. The semiconductor layers PL2 and NL2 are provided with contacts C9 and C10 for an output from the third stage, respectively, from which an output is introduced through a poly-silicon portion PS toward the next stage. A

strangulation portion S1 is provided between the contacts C1 and C5 in the semiconductor layer PL1, and a strangulation portion S3 is provided between the contacts C2 and C6 in the semiconductor layer NL1. A strangulation portion S2 is provided between contacts C7 and C9 in the semiconductor layers PL2, and a strangulation portion S4 is provided between contacts C8 and C10 in the semiconductor layer NL2. These strangulation means S1 and S3 limit an electric current of the output of inverter I2, and it simultaneously decreases parasitic capacity of a transistor included in the inverter I2 by decreasing electric currency. (col. 2, line 44 through col. 3, line 8)

Thus, *Shou et al* is merely directed to a method of forming a circuit of a plurality of MOS inverters. Nothing in *Shou et al* shows, teaches or suggests a current/leakage prevention portion for preventing current leakage as claimed in claims 13 and 19 and new claims 25 and 31. Rather, *Shou et al* never mentions preventing current leakage.

Also, *Shou et al* merely discloses an active region PL1 having a strangulation region S1 and including a first gate electrode G disposed between contacts C3, C1, and a second gate electrode G disposed between contacts C1, C5. Nothing in *Shou et al* shows, teaches or suggests a) a length of a first edge is greater than a length of a second edge and a second gate electrode beyond a third edge is defined by having a second length from the third edge to the first edge, the second length being greater than a first length of a first gate electrode from a fourth edge to a first end thereof as claimed in claims 13 and 19, and b) first and second gate electrodes are disposed directly adjacent to each other as claimed in new claims 25 and 31.

*Bergemont* appears to disclose, according to conventional single poly integrated circuit fabrication techniques, all of the polysilicon lines in the circuit are defined simultaneously utilizing a single mask step. That is, a layer of polysilicon (poly1) is first formed over the entire device structure. A poly 1 photoresist mask is then formed and pattern to define the underlying polysilicon. A single etch step is then performed to define individual poly1 lines. As shown in Fig. 1A, the fabrication process specification defines the desired offset distances "a" and "b" for the "end caps" of the individual polysilicon lines in both the x-direction and the y-direction, respectively. However, rather than the substantially rectangular ($90^0$) geometry shown in Fig. 1A, in reality, the final geometry of both the field oxide island 10 and the end cap of the polysilicon line 12 is more "rounded", as shown in Fig. 1B. The field oxide rounding effect is inherent to the type of field isolation and photolithographic process used. The poly end cap rounding effect is inherent to the photolithography of small polysilicon lines. As shown in Fig. 1B, these physical rounding effects result in a reduced width of the polysilicon lines 10 at the poly1/field oxide interface. Thus, when the poly1 line is used as a self-aligned mask for the implementation of dopant to create the source and drain regions of MOS transistors in the circuit, the channel length of the MOS device is reduced, leading to undesirable current leakage from one side of the poly1 to the other. Any misalignment of the poly1 mask further exacerbates this leakage problem, as shown in Fig. 1C. To avoid this problem, prior art techniques rely on larger design rules. That is, design rules for the length of the poly end cap, the distance between the poly end cap and the parallel edge of the field oxide, and the width of the poly1 line all may be increased. These steps insure that the channel length of each of the MOS

devices in the circuit is greater than an acceptable minimum required to prevent leakage.

Thus, *Bergemont* merely discloses desired offset distances for different individual end caps in the X and Y directions. Nothing in *Bergemont* shows, teaches or suggests a) a length of the first edge is greater than a length of a second edge and that the length of the second gate electrode from the third edge to a first end thereof is greater than the length of the first gate electrode from the fourth edge to a first end thereof as claimed in claims 13 and 19 or b) the first and second gate electrodes are directly disposed adjacent to each other as claimed in new claims 25 and 31. Rather, *Bergemont* merely discloses offset distances for individual end caps in the X and Y directions.

The combination of *Shou et al.* and *Bergemont* would merely suggest that each gates of *Shou et al.* is provided with an end cap having the desired offset directions in the X and Y directions as taught by *Bergemont*. Thus, nothing in the combination of *Shou et al.* and *Bergemont* shows, teaches or suggests the features as claimed in claims 13 and 19 or new claims 25 and 31. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 13 and 19 under 35 U.S.C. §103 and allows new claims 25-36.

Claims 17-18, 23 and 24 depend from claims 13 and 19 and recite additional features. Applicants respectfully submit that claims 17-18 and 23-24 would not have been obvious within the meaning of 35 U.S.C. §103 over *Shou et al.* and *Bergemont* at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 17-18 and 23-24 under 35 U.S.C. §103.

Claims 14-16 and 20-22 were rejected under 35 U.S.C. §103 as being unpatentable over *Shou et al.*, *Bergemont* and further in view of *Jassowski et al.* (U.S. Patent No. 5,668,389).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will set forth below, Applicants respectfully request the Examiner withdraws the rejection to the claims and allows the claims to issue.

As discussed above, since nothing in the combination of *Shou et al.* and *Bergemont* shows, teaches or suggests the primary features as claimed in claims 13 and 19, Applicants respectfully submit that the combination of the primary references with the secondary reference to *Jassowski et al.* will not overcome the deficiencies of the primary reference. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 14-16 and 20-22 under 35 U.S.C. §103.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

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By: Ellen Marcie Emas, RN28632
for Ellen Marcie Emas
Registration No. 32,131

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620